WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

2. A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein a sidewall film is formed on the surfaces of the sides of

said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

3. A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

4. A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said sputter etching is Ar sputter etching.

5. A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said metal film is a film of Co.

6. A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said MISFETs configure an SRAM memory cell.

7. A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

8. A method of fabricating a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film and where said gate electrode are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

9. A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein a sidewall film is formed on the surfaces of the sides of

said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

10. A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

11. A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said sputter etching is Ar sputter etching.

12. A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said metal film is a film of Co.

13. A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said MISFETs configure an SRAM memory cell.

14. A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

15. A method of fabricating a semiconductor integrated circuit device and has MISFETs formed on the main surface of a semiconductor substrate which has a standby current of 1.5 μA or below in actual operation, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

16. A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

17. A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

18. A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said sputter etching is Ar sputter etching.

19. A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said metal film is a film of Co.

20. A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said MISFETs configure an SRAM memory cell.

21. A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

22. A method of fabricating a semiconductor integrated circuit device that has a standby current of 1.5 μA or

below in actual operation and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film and where said gate electrode are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

23. A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

24. A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

25. A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said sputter etching is Ar sputter etching.

26. A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said metal film is a film of Co.

27. A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said MISFETs configure an SRAM memory cell.

28. A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

29. A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

30. A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

31. A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

32. A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said sputter etching is Ar sputter etching.

33. A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said metal film is a film of Co.

34. A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said MISFETs configure an SRAM memory cell.

35. A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

36. A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film and where said gate electrode are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

37. A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

38. A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

39. A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said sputter etching is Ar sputter etching.

40. A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said metal film is a film of Co.

41. A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said MISFETs configure an SRAM memory cell.

42. A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

43. A method of fabricating a semiconductor integrated circuit device that has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer with a thickness of 20 to 40 nm where said source/drain regions are in contact with said metallic film; and

(g) removing that part of said metal film which did not react in step (f).

44. A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

45. A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

46. A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said sputter etching is Ar sputter etching.

47. A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said metal film is a film of Co.

48. A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said MISFETs configure an SRAM memory cell.

49. A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

50. A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain regions and on said gate electrode to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer with a thickness of 20 to 40 nm where said source/drain regions are in contact with said metallic film and where said gate electrode are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

51. A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

52. A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

53. A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said sputter etching is Ar sputter etching.

54. A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said metal film is a film of Co.

55. A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said MISFETs configure an SRAM memory cell.

56. A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

57. A method of fabricating a semiconductor integrated circuit device that has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain

regions to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer with sheet resistance of 5Ω/□ to 12Ω/□, where said source/drain regions are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

58. A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

59. A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

60. A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said sputter etching is Ar sputter etching.

61. A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said metal film is a film of Co.

62. A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said MISFETs configure an SRAM memory cell.

63. A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

64. A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said source/drain

regions and on said gate electrode to 2.5 nm or less below the surface of the regions;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer with sheet resistance of 5Ω/□ to 12Ω/□, where said source/drain regions are in contact with said metal film and where said gate electrode are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

65. A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein a sidewall film is formed on the surfaces of the sides of said gate electrode and said source/drain regions are then formed by using the sidewall film as a mask.

66. A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said sputter etching is carried out after the surface of said source/drain regions has been cleaned by using hydrofluoric acid as a cleaning agent.

67. A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said sputter etching is Ar sputter etching.

68. A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said metal film is a film of Co.

69. A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said MISFETs configure an SRAM memory cell.

70. A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein a metal film is formed on said source/drain regions, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.